

CD4069UB CMOS 六路逆变器

1 特性

- 标准化对称输出特性
- 中速运行: t_{PHL} 、 $t_{\text{PLH}} = 30\text{ns}$, 10V (典型值)
- 100% 测试 20V 时的静态电流
- 在全封装温度范围内, 在 18V 时的最大输入电流为 $1\mu\text{A}$, 在 18V 和 25°C 时为 100nA
- 符合 JEDEC 第 13B 号暂行标准, 《B 系列 CMOS 器件 说明规范标准》的所有要求

2 应用

- 逻辑反相
- 脉冲整形
- 振荡器
- 高输入阻抗放大器

3 说明

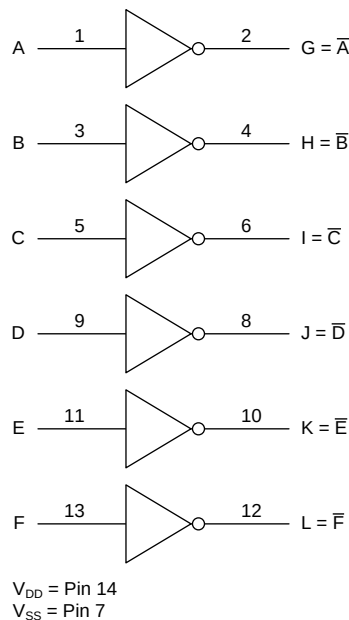
CD4069UB 器件由六个 CMOS 逆变器电路组成。这些器件可用于所有不需要电路中功耗 TTL 驱动和逻辑电平转换功能的通用逆变器应用, 例如 CD4009 和 CD4049 六路逆变器和缓冲器。

器件信息⁽¹⁾

器件型号	封装 (引脚)	封装尺寸 (标称值)
CD4069UBE	PDIP (14)	19.30mm x 6.35mm
CD4069UBF	CDIP (14)	19.56mm x 6.67mm
CD4069UBM	SOIC (14)	8.65mm x 3.91mm
CD4069UBNSR	SO (14)	10.30mm x 5.30mm
CD4069UBPW	TSSOP (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

CD4069UB 功能框图



目录

1	特性	1	8.3	Feature Description	13
2	应用	1	8.4	Device Functional Modes	13
3	说明	1	9	Application and Implementation	14
4	修订历史记录	2	9.1	Application Information	14
5	Pin Configuration and Functions	3	9.2	Typical Application	14
6	Specifications	4	10	Power Supply Recommendations	16
6.1	Absolute Maximum Ratings	4	11	Layout	16
6.2	ESD Ratings	4	11.1	Layout Guidelines	16
6.3	Recommended Operating Conditions	4	11.2	Layout Example	16
6.4	Thermal Information	4	12	器件和文档支持	17
6.5	Electrical Characteristics – Dynamic	5	12.1	器件支持	17
6.6	Electrical Characteristics – Static	5	12.2	文档支持	17
6.7	Typical Characteristics	8	12.3	社区资源	17
7	Parameter Measurement Information	9	12.4	商标	17
8	Detailed Description	13	12.5	静电放电警告	17
8.1	Overview	13	12.6	术语表	17
8.2	Functional Block Diagram	13	13	机械、封装和可订购信息	17

4 修订历史记录

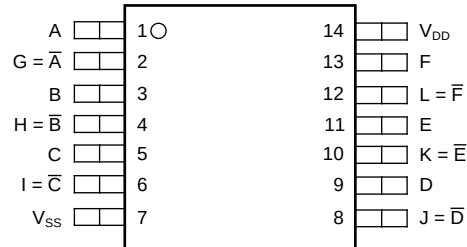
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (February 2016) to Revision E	Page
• 删除了“特性”部分第二条 t_{PHL} 处的“-”	1
• Corrected V_I spec MIN/MAX values in the Abs Max Ratings table	4
• Corrected parameter I_{DD} max term to I_{DD} in the Elec Characteristics table	5
• Corrected parameter I_{OL} min term to I_{OL} in the Elec Characteristics table	5
• Corrected parameter V_{OL} max term to V_{OL} in the Elec Characteristics table	6
• Corrected parameter V_{IL} max term to V_{IL} in the Elec Characteristics table	6
• Corrected parameter V_{IH} min term to V_{IH} in the Elec Characteristics table	6
• Corrected parameter I_{IN} max term to I_{IN} in the Elec Characteristics table	7
• Added Y-axis label to Figure 1 image object	8
• Changed text string from “ $-t_{PHL}$ ” to “of t_{PHL} ” in the Feature Description paragraph.	13

Changes from Revision C (August 2003) to Revision D	Page
• 添加了 ESD 额定值表、特性说明部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1

5 Pin Configuration and Functions

D, J, N, NS, and PW Packages
14-Pin PDIP, CDIP, SOIC, SO, and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	A input
B	3	I	B input
C	5	I	C input
D	9	I	D input
E	11	I	E input
F	13	I	F input
$G = \bar{A}$	2	O	G output
$H = \bar{B}$	4	O	H output
$I = \bar{C}$	6	O	I output
$J = \bar{D}$	8	O	J output
$K = \bar{E}$	10	O	K output
$L = \bar{F}$	12	O	L output
V_{DD}	14	—	Positive supply
V_{SS}	7	—	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{DD}	DC supply-voltage (voltages referenced to V _{SS} terminal)		−0.5	20	V
V _I	Input voltage, all inputs		−0.5	V _{DD} + 0.5	V
I _{IK}	DC input current, any one input		−10	10	mA
P _D	Power dissipation per package	−55°C to 100°C	500		mW
		100°C to 125°C	12 200		
	Device dissipation per output transistor	Full range (all package types)		100	
Lead temperature ⁽²⁾			265		°C
T _J	Junction temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) During soldering at distance 1/16 inch ± 1/32 inch (1.59 mm ± 0.79 mm) from case for 10 s maximum

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{DD}	Supply voltage	3	18	V
T _A	Operating temperature	−55	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD4069UB					UNIT
		D (SOIC)	J (CDIP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	94.9	—	57.9	91.2	122.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.4	28.5	45.5	48.8	50.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.2	—	37.7	50	63.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	21.1	—	30.6	15	6.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	48.9	—	37.6	49.6	63.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics – Dynamic

 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	$V_{DD} (V) = 5$		55	110	ns
	$V_{DD} (V) = 10$		30	60	
	$V_{DD} (V) = 15$		25	50	
t_{THL}, t_{TLH} Transition time	$V_{DD} (V) = 5$		100	200	ns
	$V_{DD} (V) = 10$		50	100	
	$V_{DD} (V) = 15$		40	80	
C_{IN} Input capacitance	Any input		10	15	pF

6.6 Electrical Characteristics – Static

 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD} Quiescent device current	$V_{IN} = 0\text{V or } 5\text{ V}, V_{DD} = 5\text{ V}$	$T_A = -55^\circ\text{C}$			0.25	μA
		$T_A = -40^\circ\text{C}$			0.25	
		$T_A = 25^\circ\text{C}$		0.01	0.25	
		$T_A = 85^\circ\text{C}$			7.5	
		$T_A = 125^\circ\text{C}$			7.5	
	$V_{IN} = 0\text{ or } 10\text{ V}, V_{DD} = 10\text{ V}$	$T_A = -55^\circ\text{C}$			0.5	
		$T_A = -40^\circ\text{C}$			0.5	
		$T_A = 25^\circ\text{C}$		0.01	0.5	
		$T_A = 85^\circ\text{C}$			15	
		$T_A = 125^\circ\text{C}$			15	
	$V_{IN} = 0\text{ or } 15\text{ V}, V_{DD} = 15\text{ V}$	$T_A = -55^\circ\text{C}$			1	
		$T_A = -40^\circ\text{C}$			1	
		$T_A = 25^\circ\text{C}$		0.01	1	
		$T_A = 85^\circ\text{C}$			30	
		$T_A = 125^\circ\text{C}$			30	
	$V_{IN} = 0\text{ or } 20\text{ V}, V_{DD} = 20\text{ V}$	$T_A = -55^\circ\text{C}$			5	
		$T_A = -40^\circ\text{C}$			5	
		$T_A = 25^\circ\text{C}$		0.02	5	
		$T_A = 85^\circ\text{C}$			150	
		$T_A = 125^\circ\text{C}$			150	
I_{OL} Output low (sink) current	$V_O = 0.4\text{ V}, V_{IN} = 5\text{ V}, V_{DD} = 5\text{ V}$	$T_A = -55^\circ\text{C}$	0.64			mA
		$T_A = -40^\circ\text{C}$	0.61			
		$T_A = 25^\circ\text{C}$	0.51	1		
		$T_A = 85^\circ\text{C}$	0.42			
		$T_A = 125^\circ\text{C}$	0.36			
	$V_O = 0.5\text{ V}, V_{IN} = 10\text{ V}, V_{DD} = 10\text{ V}$	$T_A = -55^\circ\text{C}$	1.6			
		$T_A = -40^\circ\text{C}$	1.5			
		$T_A = 25^\circ\text{C}$	1.3	2.6		
		$T_A = 85^\circ\text{C}$	1.1			
		$T_A = 125^\circ\text{C}$	0.9			
	$V_O = 1.5\text{ V}, V_{IN} = 15\text{ V}, V_{DD} = 15\text{ V}$	$T_A = -55^\circ\text{C}$	4.2			
		$T_A = -40^\circ\text{C}$	4			
		$T_A = 25^\circ\text{C}$	3.4	6.8		
		$T_A = 85^\circ\text{C}$	2.8			
		$T_A = 125^\circ\text{C}$	2.4			

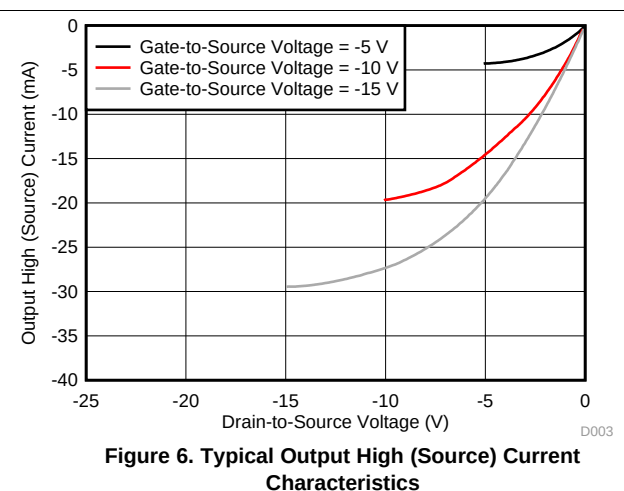
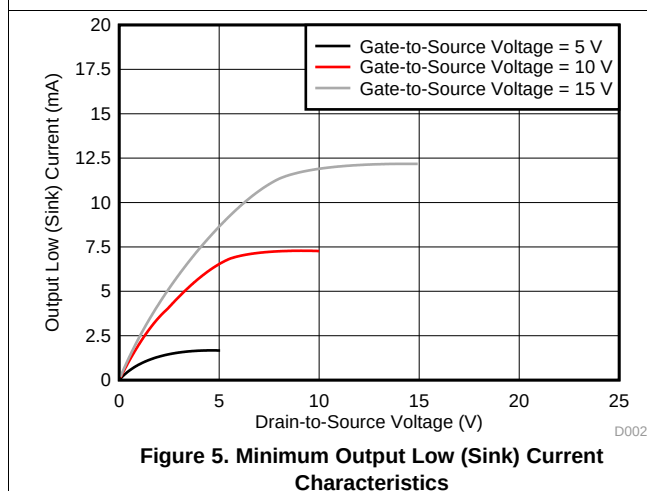
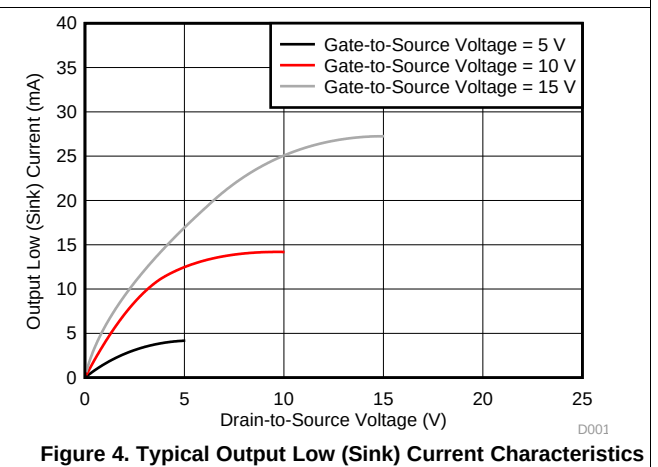
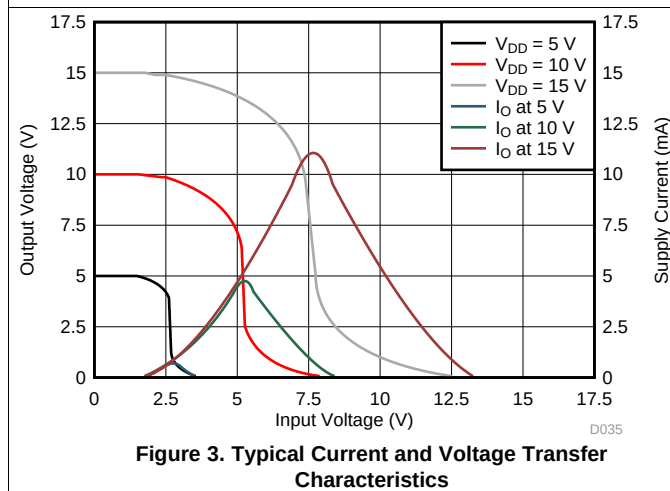
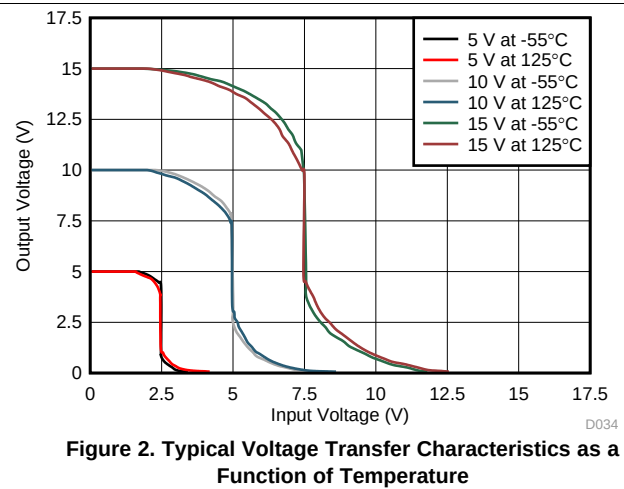
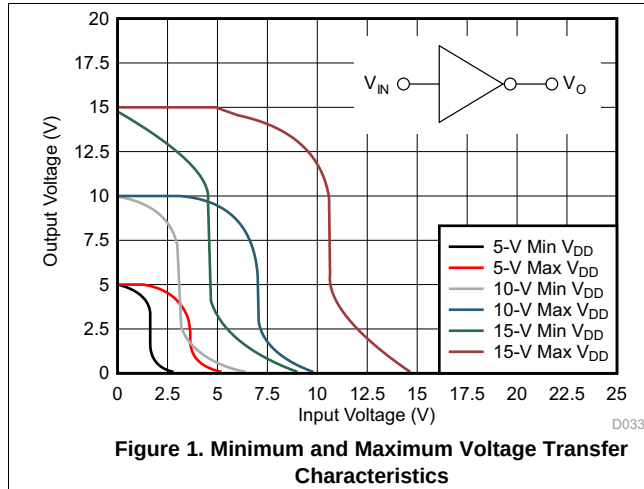
Electrical Characteristics – Static (continued)
 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH} Output high (source) current	$V_O = 4.6\text{ V}, V_{IN} = 0\text{ V}, V_{DD} = 5\text{ V}$	$T_A = -55^\circ\text{C}$		-0.64	mA
		$T_A = -40^\circ\text{C}$		-0.61	
		$T_A = 25^\circ\text{C}$	-1	-0.51	
		$T_A = 85^\circ\text{C}$		-0.42	
		$T_A = 125^\circ\text{C}$		-0.36	
	$V_O = 2.5\text{ V}, V_{IN} = 0\text{ V}, V_{DD} = 5\text{ V}$	$T_A = -55^\circ\text{C}$		-2	
		$T_A = -40^\circ\text{C}$		-1.8	
		$T_A = 25^\circ\text{C}$	-3.2	-1.6	
		$T_A = 85^\circ\text{C}$		-1.3	
		$T_A = 125^\circ\text{C}$		-1.15	
	$V_O = 9.5\text{ V}, V_{IN} = 0\text{ V}, V_{DD} = 10\text{ V}$	$T_A = -55^\circ\text{C}$		-1.6	
		$T_A = -40^\circ\text{C}$		-1.5	
		$T_A = 25^\circ\text{C}$	-2.6	-1.3	
		$T_A = 85^\circ\text{C}$		-1.1	
		$T_A = 125^\circ\text{C}$		-0.9	
	$V_O = 13.5\text{ V}, V_{IN} = 0\text{ V}, V_{DD} = 15\text{ V}$	$T_A = -55^\circ\text{C}$		-4.2	
		$T_A = -40^\circ\text{C}$		-4	
		$T_A = 25^\circ\text{C}$	-6.8	-3.4	
		$T_A = 85^\circ\text{C}$		-2.8	
		$T_A = 125^\circ\text{C}$		-2.4	
V_{OL} Low-level output voltage	$V_{IN} = 5\text{ V}, V_{DD} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	0	0.05	V
		All other temperatures		0.05	
	$V_{IN} = 10\text{ V}, V_{DD} = 10\text{ V}$	$T_A = 25^\circ\text{C}$	0	0.05	
		All other temperatures		0.05	
	$V_{IN} = 15\text{ V}, V_{DD} = 15\text{ V}$	$T_A = 25^\circ\text{C}$	0	0.05	
		All other temperatures		0.05	
V_{OH} High-level output voltage	$V_{IN} = 0\text{ V}, V_{DD} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	4.95	5	V
		All other temperatures	4.95		
	$V_{IN} = 0\text{ V}, V_{DD} = 10\text{ V}$	$T_A = 25^\circ\text{C}$	9.95	10	
		All other temperatures	9.95		
	$V_{IN} = 0\text{ V}, V_{DD} = 15\text{ V}$	$T_A = 25^\circ\text{C}$	14.95	15	
		All other temperatures	14.95		
V_{IL} Input low voltage	$V_O = 4.5\text{ V}, V_{DD} = 5\text{ V}, \text{all temperatures}$			1	V
	$V_O = 9\text{ V}, V_{DD} = 10\text{ V}, \text{all temperatures}$			2	
	$V_O = 13.5\text{ V}, V_{DD} = 15\text{ V}, \text{all temperatures}$			2.5	
V_{IH} Input high voltage	$V_O = 0.5\text{ V}, V_{DD} = 5\text{ V}, \text{all temperatures}$		4		V
	$V_O = 1\text{ V}, V_{DD} = 10\text{ V}, \text{all temperatures}$		8		
	$V_O = 1.5\text{ V}, V_{DD} = 15\text{ V}, \text{all temperatures}$		12.5		

Electrical Characteristics – Static (continued)
 $T_A = 25^\circ\text{C}$; input $t_r, t_f = 20\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IN} Input current	$V_{IN} = 0\text{ V to } 18\text{ V}, V_{DD} = 18\text{ V}$	$T_A = -55^\circ\text{C}$			± 01	μA
		$T_A = -40^\circ\text{C}$			± 01	
		$T_A = 25^\circ\text{C}$		$\pm 10^{-5}$	± 1	
		$T_A = 85^\circ\text{C}$			± 1	
		$T_A = 125^\circ\text{C}$			± 1	

6.7 Typical Characteristics



Typical Characteristics (continued)

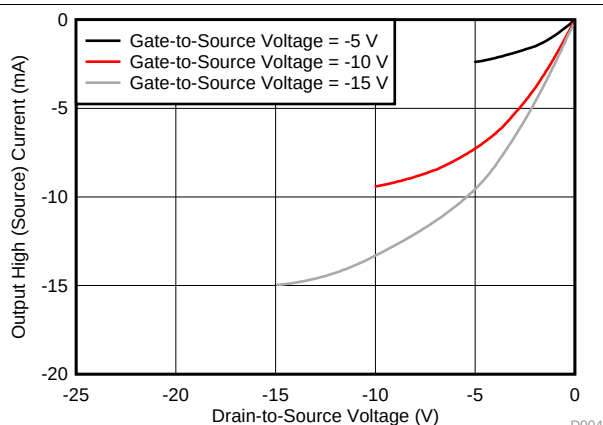


Figure 7. Minimum Output High (Source) Current Characteristics

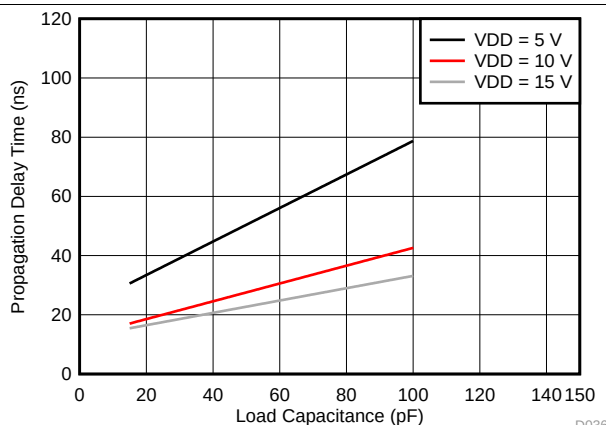


Figure 8. Typical Propagation Delay Time vs Load Capacitance

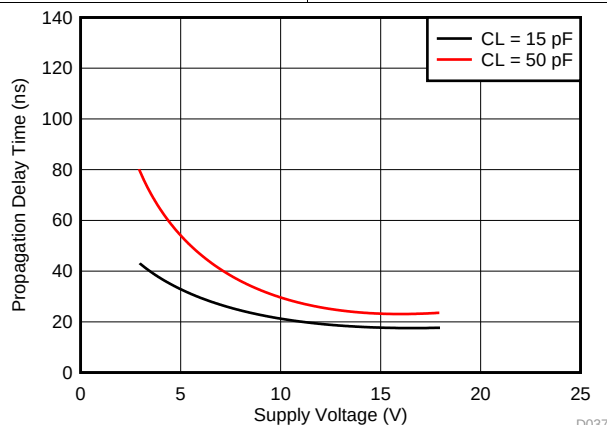


Figure 9. Typical Propagation Delay Time vs Supply Voltage

7 Parameter Measurement Information

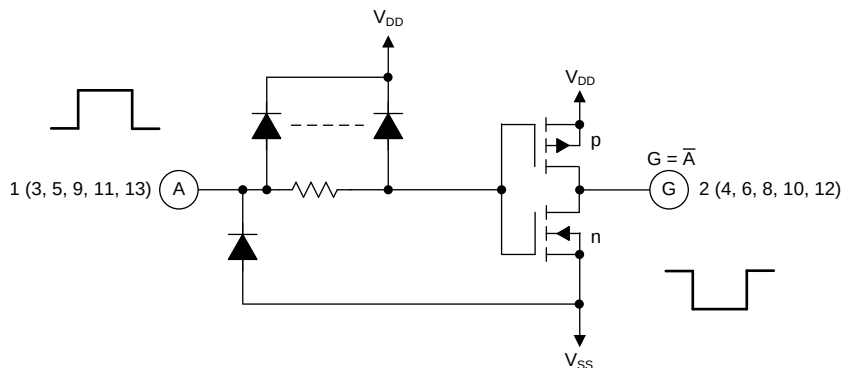


Figure 10. Schematic Diagram of One of Six Identical Inverters

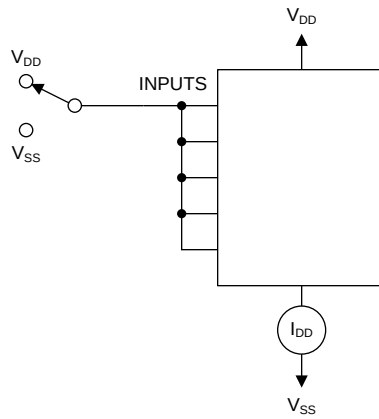


Figure 11. Quiescent Device Current Test Circuit

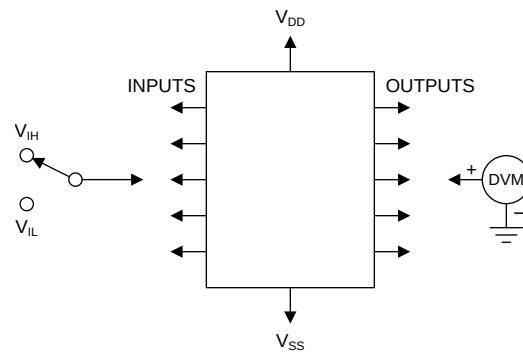


Figure 12. Noise Immunity Test Circuit

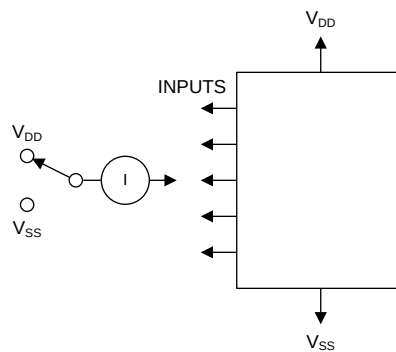


Figure 13. Input Leakage Current Test Circuit

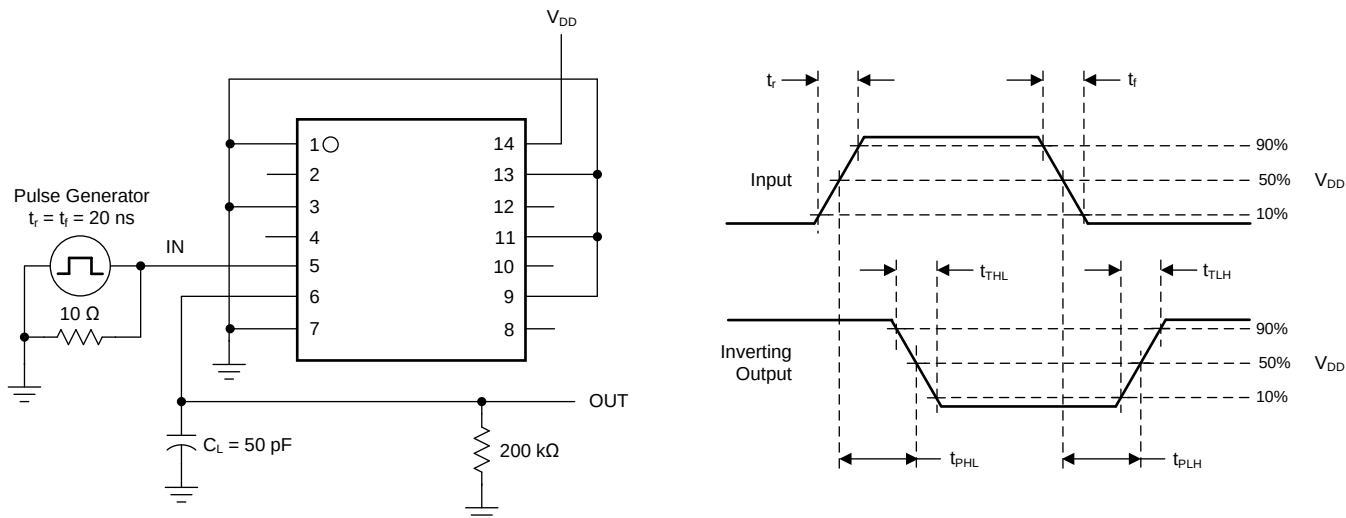


Figure 14. Dynamic Electrical Characteristics Test Circuit and Waveform

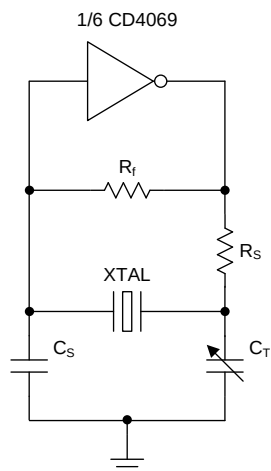


Figure 15. Typical Crystal Oscillator Circuit

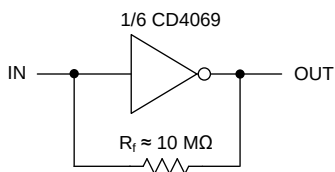


Figure 16. High-Input Impedance Amplifier

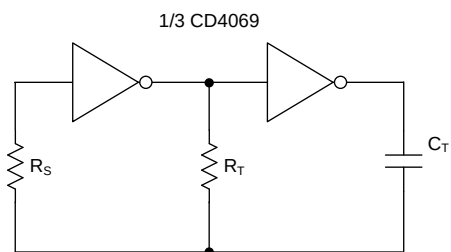


Figure 17. Typical RC Oscillator Circuit

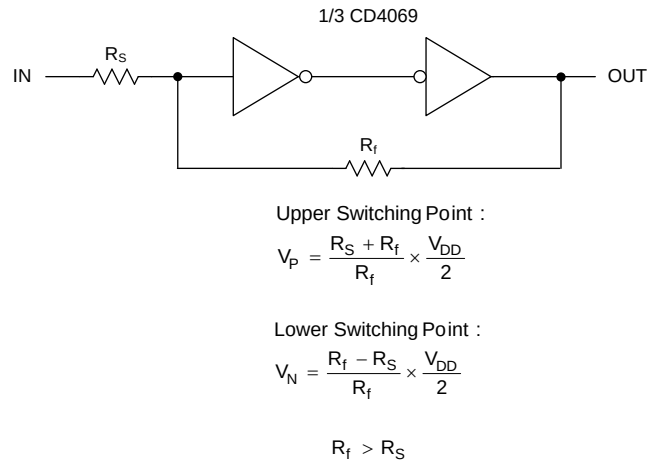


Figure 18. Input Pulse Shaping Circuit

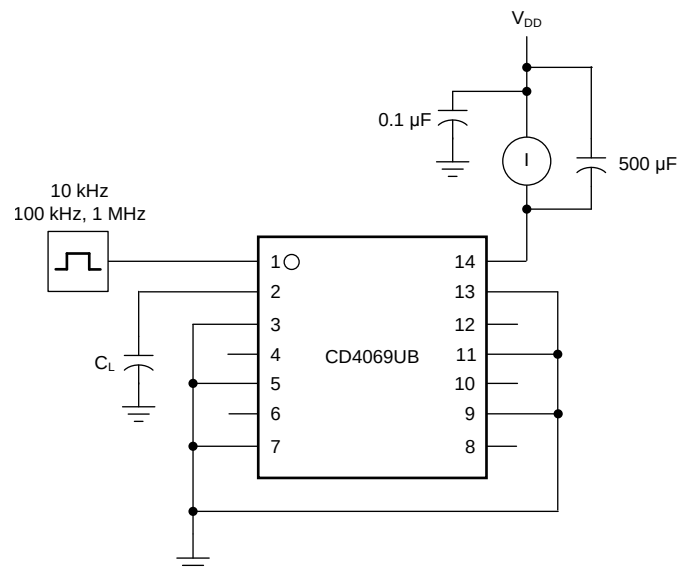


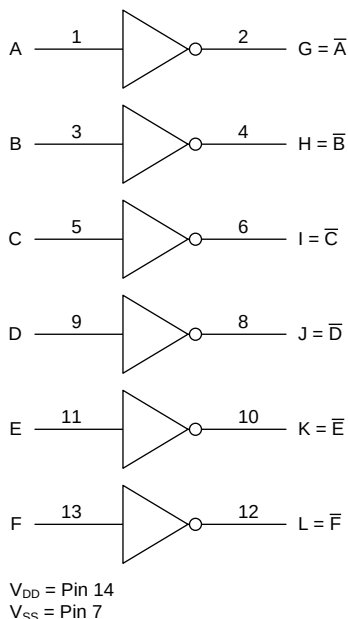
Figure 19. Dynamic Power Dissipation Test Circuit

8 Detailed Description

8.1 Overview

The CD4069UB device has six inverter circuits. The recommended operating range is from 3 V to 18 V. The CD4069UB-series types are supplied in 14-pin hermetic dual-in-line ceramic packages (F3A suffix), 14-pin dual-in-line plastic packages (E suffix), 14-pin small-outline packages (M, MT, M96, and NSR suffixes), and 14-pin thin shrink small-outline packages (PW and PWR suffixes).

8.2 Functional Block Diagram



8.3 Feature Description

CD4069UB has standardized symmetrical output characteristics and a wide operating voltage range from 3 V to 18 V with quiescent current tested at 20 V. This has a medium operation speed of t_{PHL} , t_{PLH} = 30 ns (typical) at 10 V. The operating temperature is from -55°C to 125°C . CD4069UB meets all requirements of JEDEC tentative standard No. 13B, *Standard Specifications for Description of B Series CMOS Devices*.

8.4 Device Functional Modes

Table 1 shows the functional modes for CD4069UB.

Table 1. Function Table

INPUT A, B, C, D, E, F	OUTPUT G, H, I, J, K, L
H	L
L	H

9 Application and Implementation

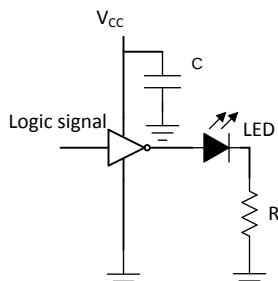
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CD4069UB device has a low input current of 1 μA at 18 V over full package-temperature range and 100 nA at 18 V, 25°C. This device has a wide operating voltage range from 3 V to 18 V and used in high voltage applications.

9.2 Typical Application



Copyright © 2016,
Texas Instruments Incorporated

Figure 20. CD4069UB Application

9.2.1 Design Requirements

The CD4069UB device is the industry's highest logic inverter operating at 18 V under recommended conditions. The lower drive capabilities makes it suitable for driving light loads like LED and greatly reduces chances of overshoots and undershoots.

9.2.2 Detailed Design Procedure

The recommended input conditions for [Figure 20](#) includes rise time and fall time specifications (see $\Delta t/\Delta V$ in [Recommended Operating Conditions](#)) and specified high and low levels (see V_{IH} and V_{IL} in [Recommended Operating Conditions](#)). Inputs are not overvoltage tolerant and must be below V_{CC} level because of the presence of input clamp diodes to V_{CC} .

The recommended output condition for the CD4069UB application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through V_{CC} or GND) for the device. These limits are located in the [Absolute Maximum Ratings](#). Outputs must not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curves

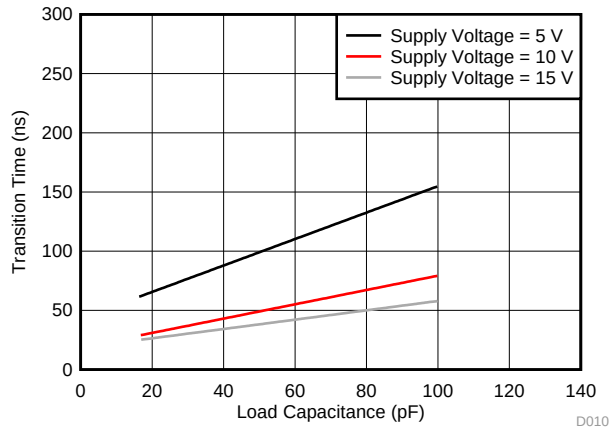


Figure 21. Typical Transition Time vs Load Capacitance

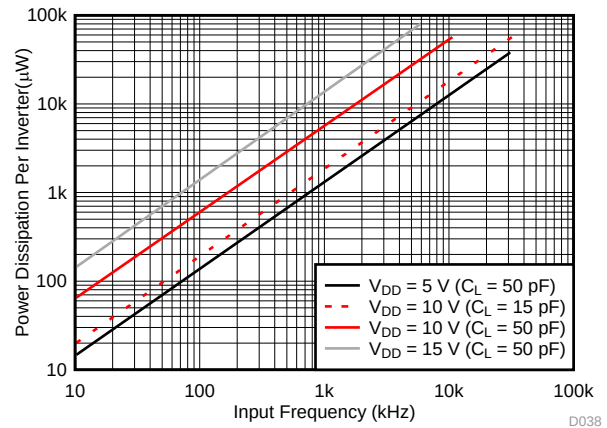


Figure 22. Typical Dynamic Power Dissipation vs Frequency

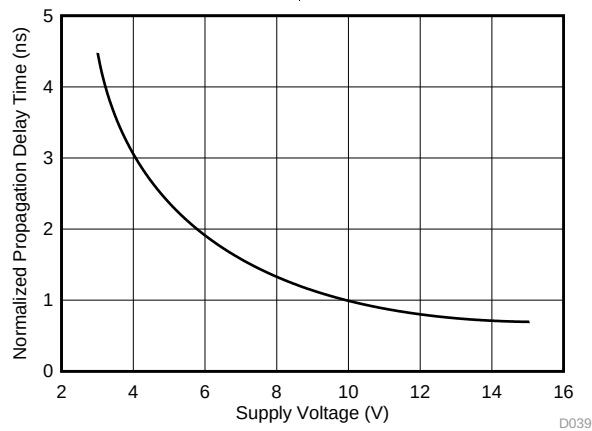


Figure 23. Variation of Normalized Propagation Delay Time (t_{PHL} and t_{PLH}) With Supply Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor. If there are multiple V_{CC} pins, then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

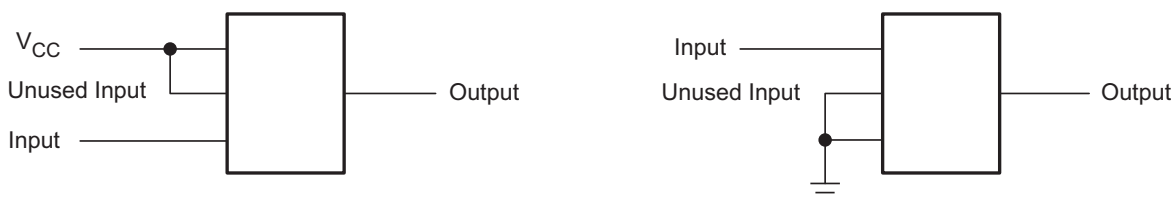
11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, digital logic device functions or parts of these functions are unused (for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. This rule must be observed under all circumstances specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. See the application note, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)), for more information on the effects of floating inputs. The logic level must apply to any particular unused input depending on the function of the device. Generally, they are tied to GND or V_{CC} (whichever is convenient).

11.2 Layout Example



12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 《CMOS 输入缓慢变化或悬空的影响》，SCBA004

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4069UBE	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4069UBE
CD4069UBE.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4069UBE
CD4069UBEE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4069UBE
CD4069UBF	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4069UBF
CD4069UBF.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4069UBF
CD4069UBF3A	NRND	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4069UBF3A
CD4069UBF3A.A	NRND	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4069UBF3A
CD4069UBM	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM
CD4069UBM.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM
CD4069UBM96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM
CD4069UBM96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UBM
CD4069UBMT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4069UBM
CD4069UBNSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UB
CD4069UBNSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4069UB
CD4069UBPW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-55 to 125	CM069UB
CD4069UBPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	CM069UB
CD4069UBPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB
CD4069UBPWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM069UB
JM38510/17401BCA	NRND	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17401BCA
JM38510/17401BCA.A	NRND	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17401BCA
M38510/17401BCA	NRND	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17401BCA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

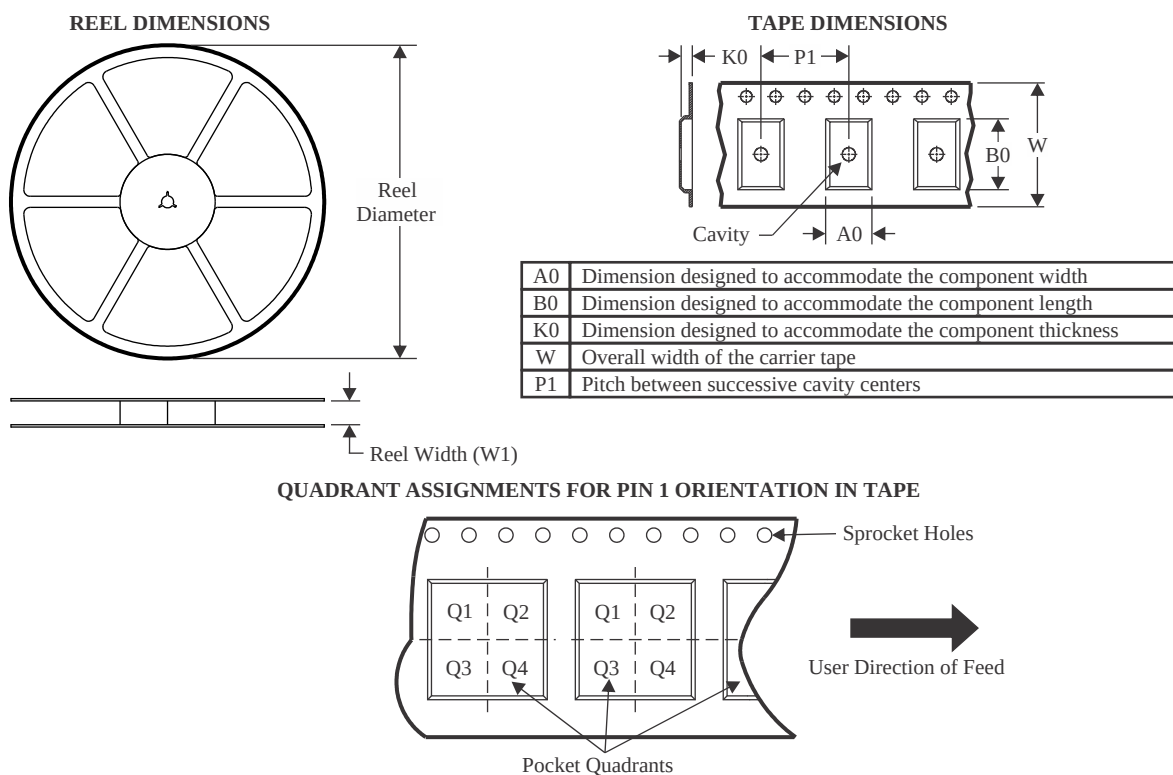
OTHER QUALIFIED VERSIONS OF CD4069UB, CD4069UB-MIL :

- Catalog : [CD4069UB](#)
- Military : [CD4069UB-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

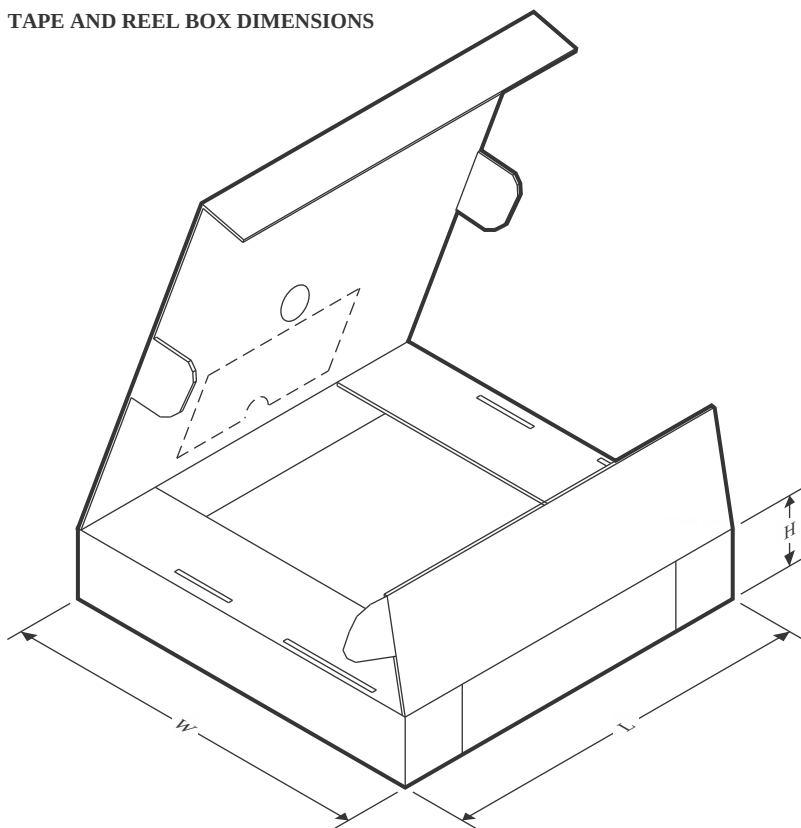
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4069UBM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4069UBNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4069UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4069UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

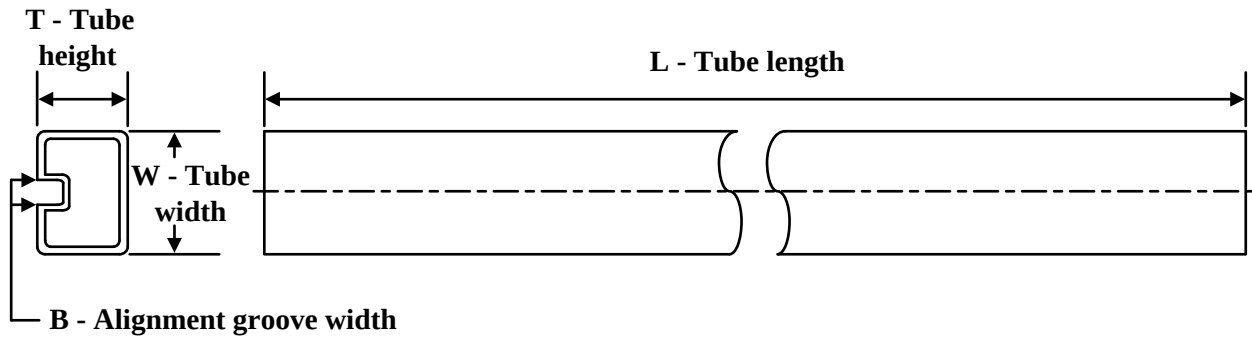
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

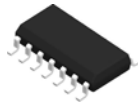
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4069UBM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4069UBNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4069UBPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
CD4069UBPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE

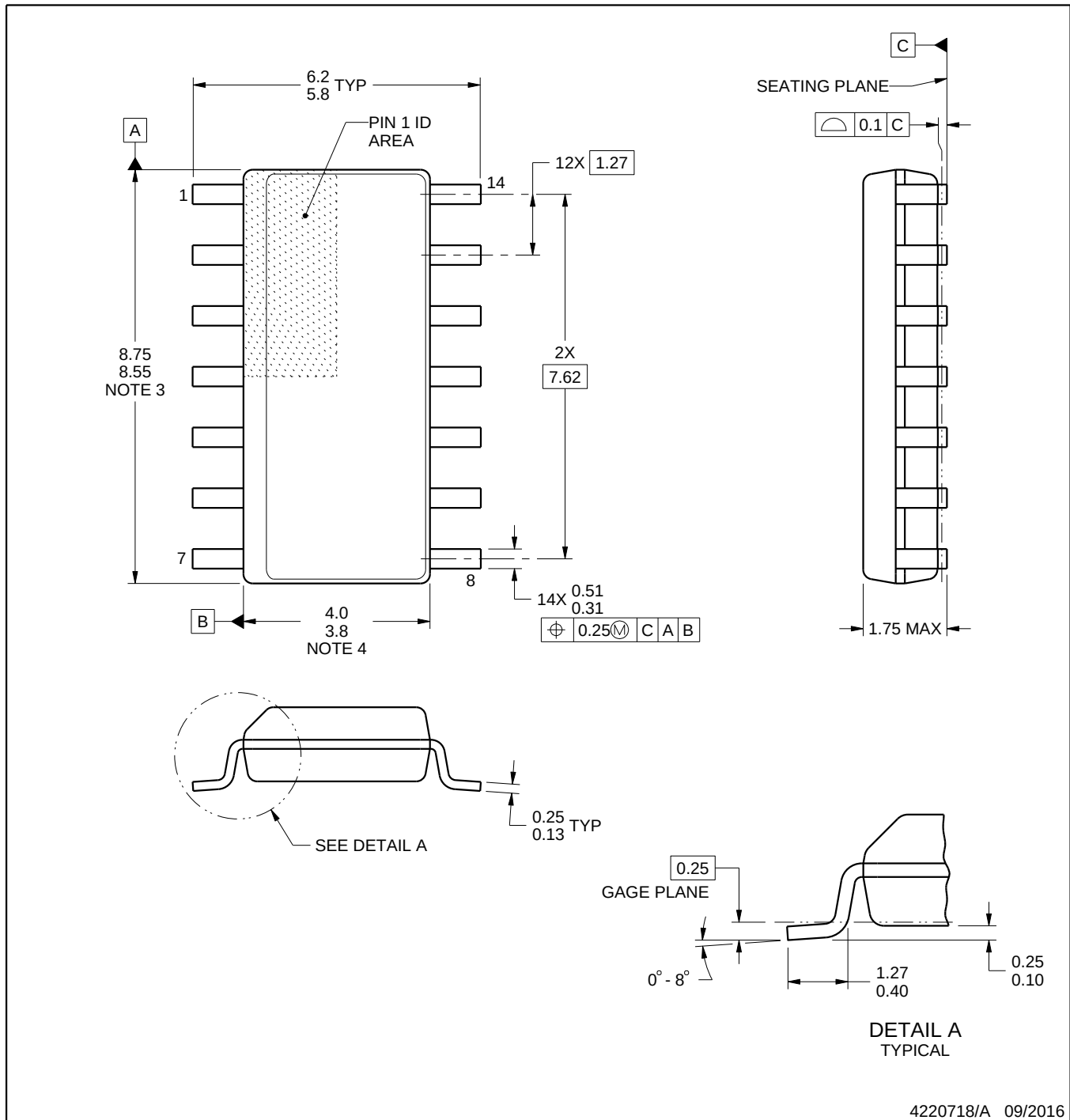


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4069UBE	N	PDIP	14	25	506	13.97	11230	4.32
CD4069UBE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4069UBEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4069UBM	D	SOIC	14	50	506.6	8	3940	4.32
CD4069UBM.A	D	SOIC	14	50	506.6	8	3940	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

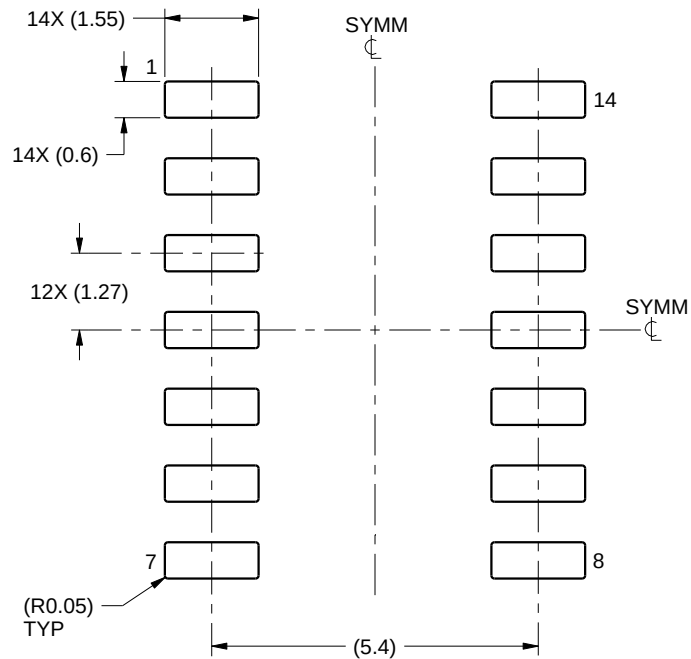
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

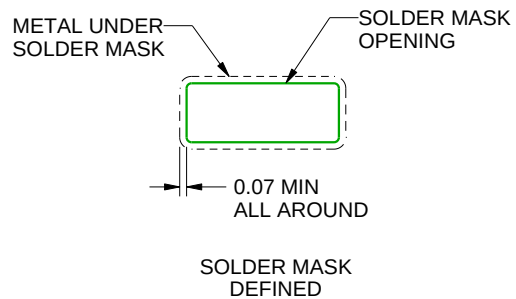
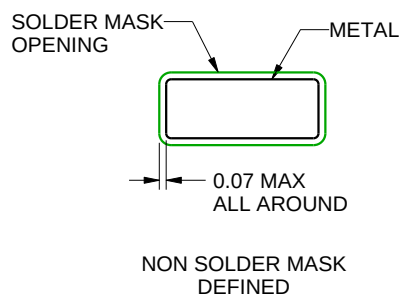
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

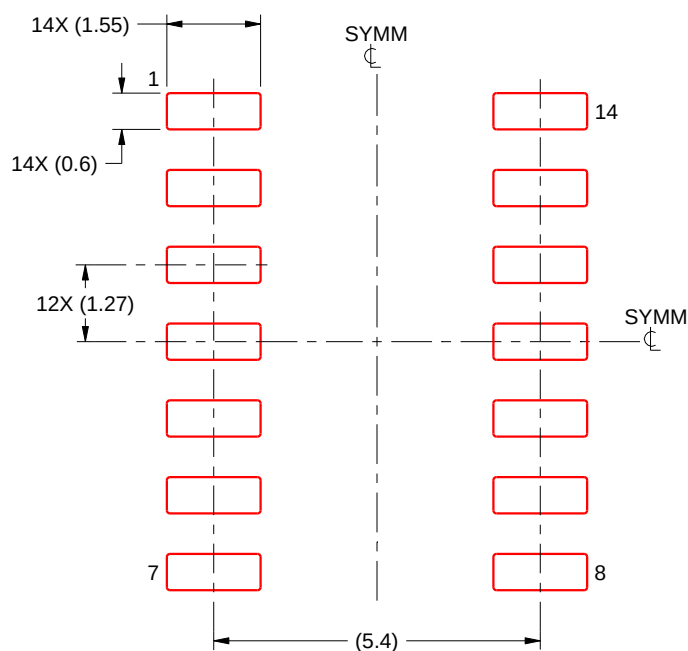
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

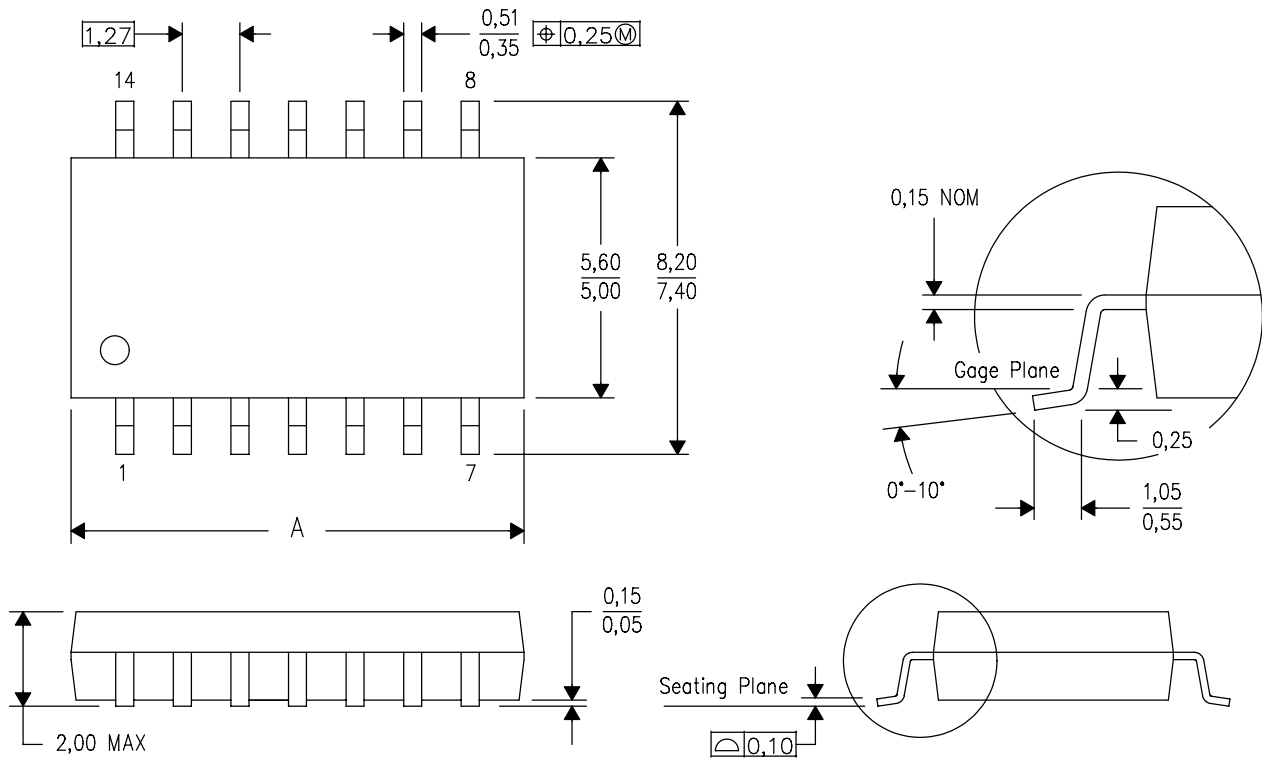
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

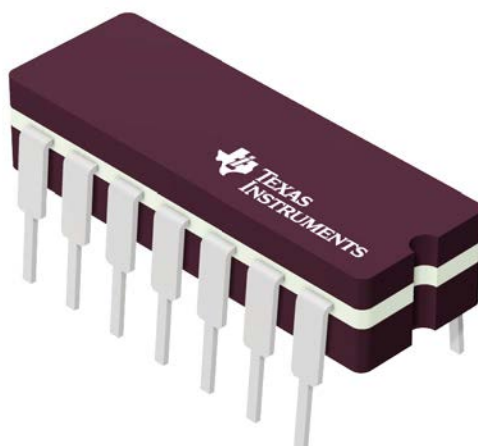
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW

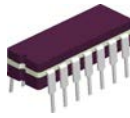
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

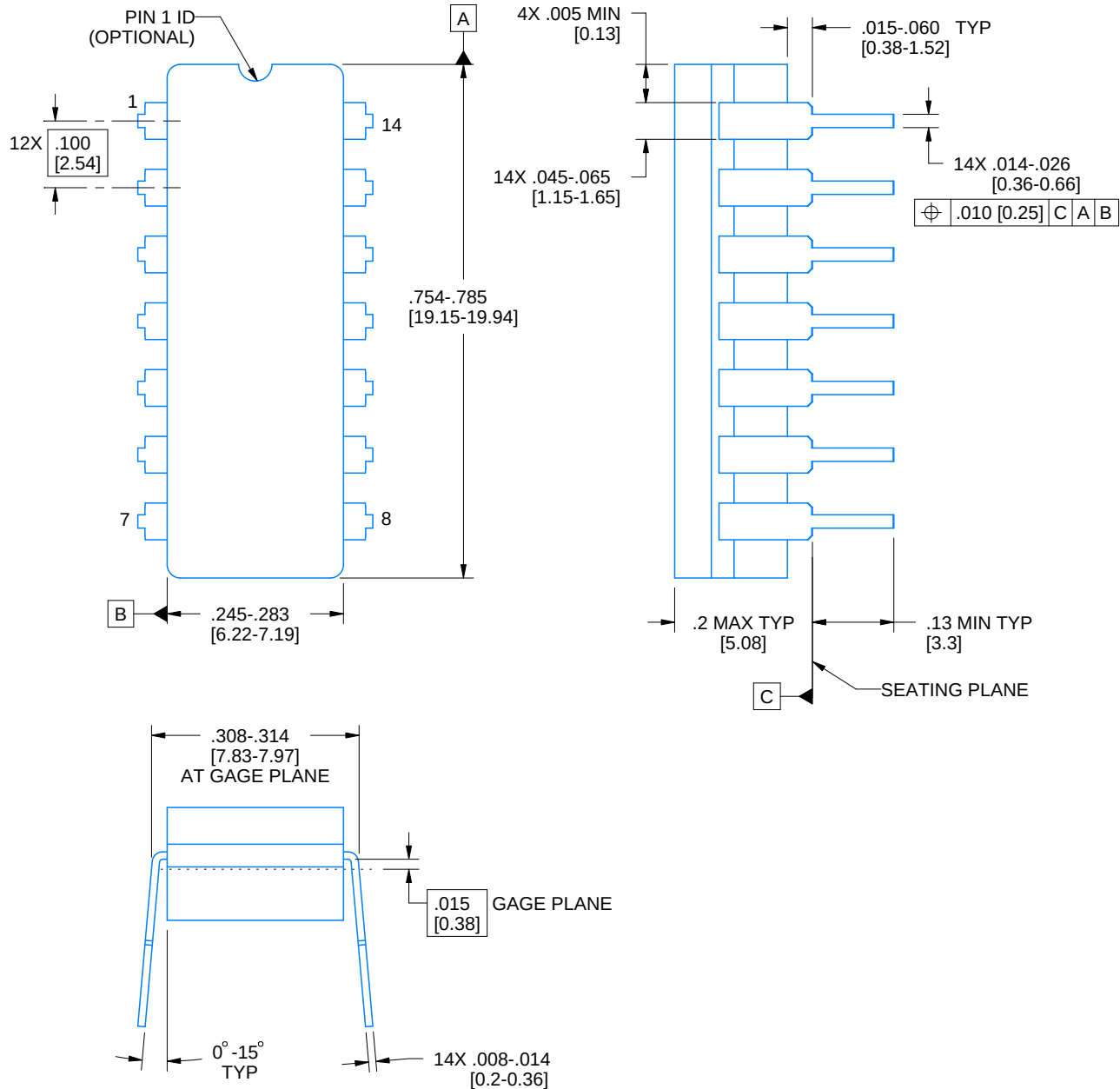


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



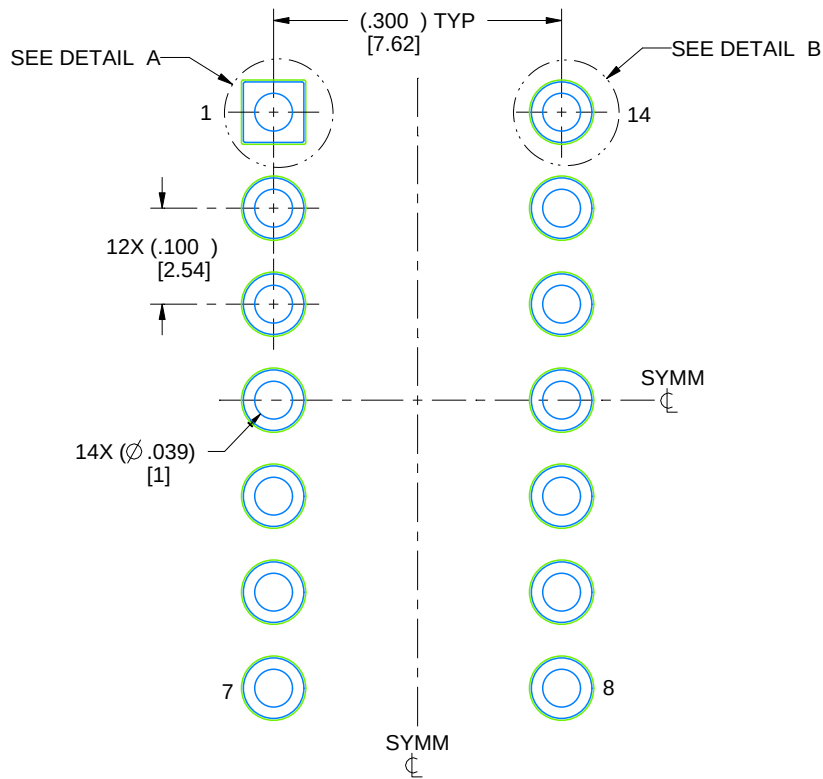
**TEXAS
INSTRUMENTS**
www.ti.com

EXAMPLE BOARD LAYOUT

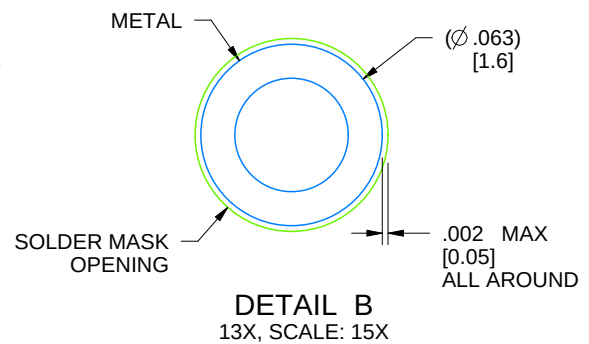
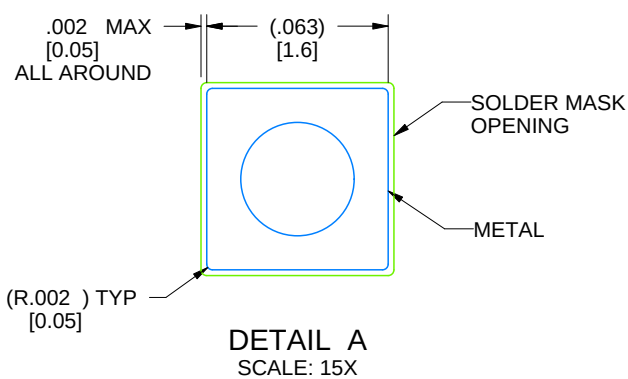
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

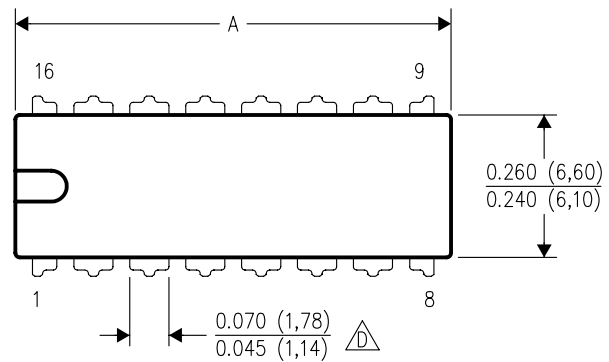


4214771/A 05/2017

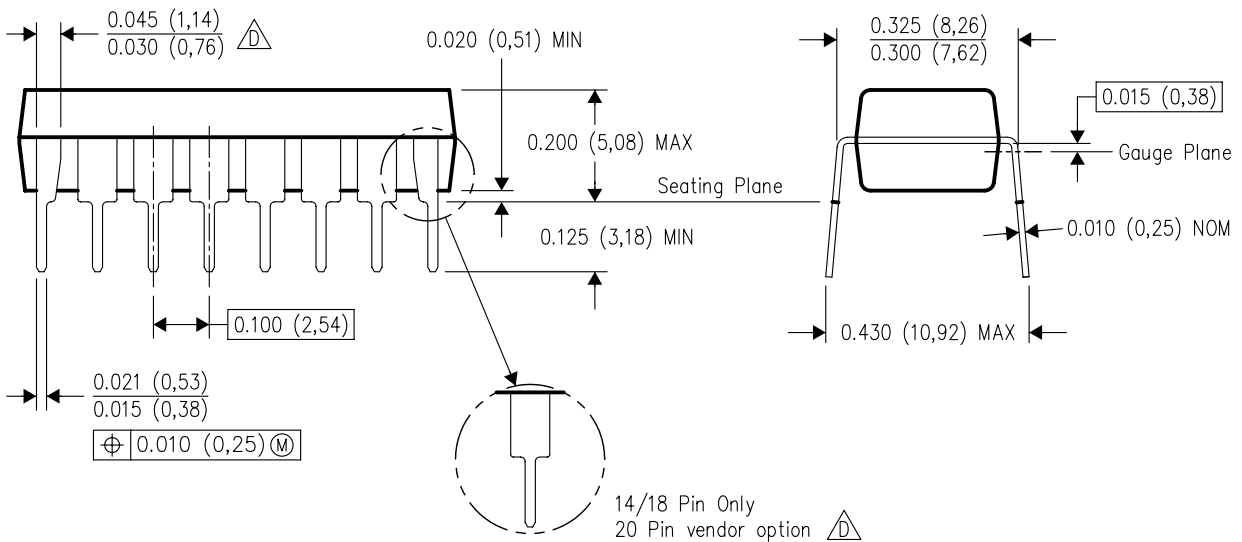
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

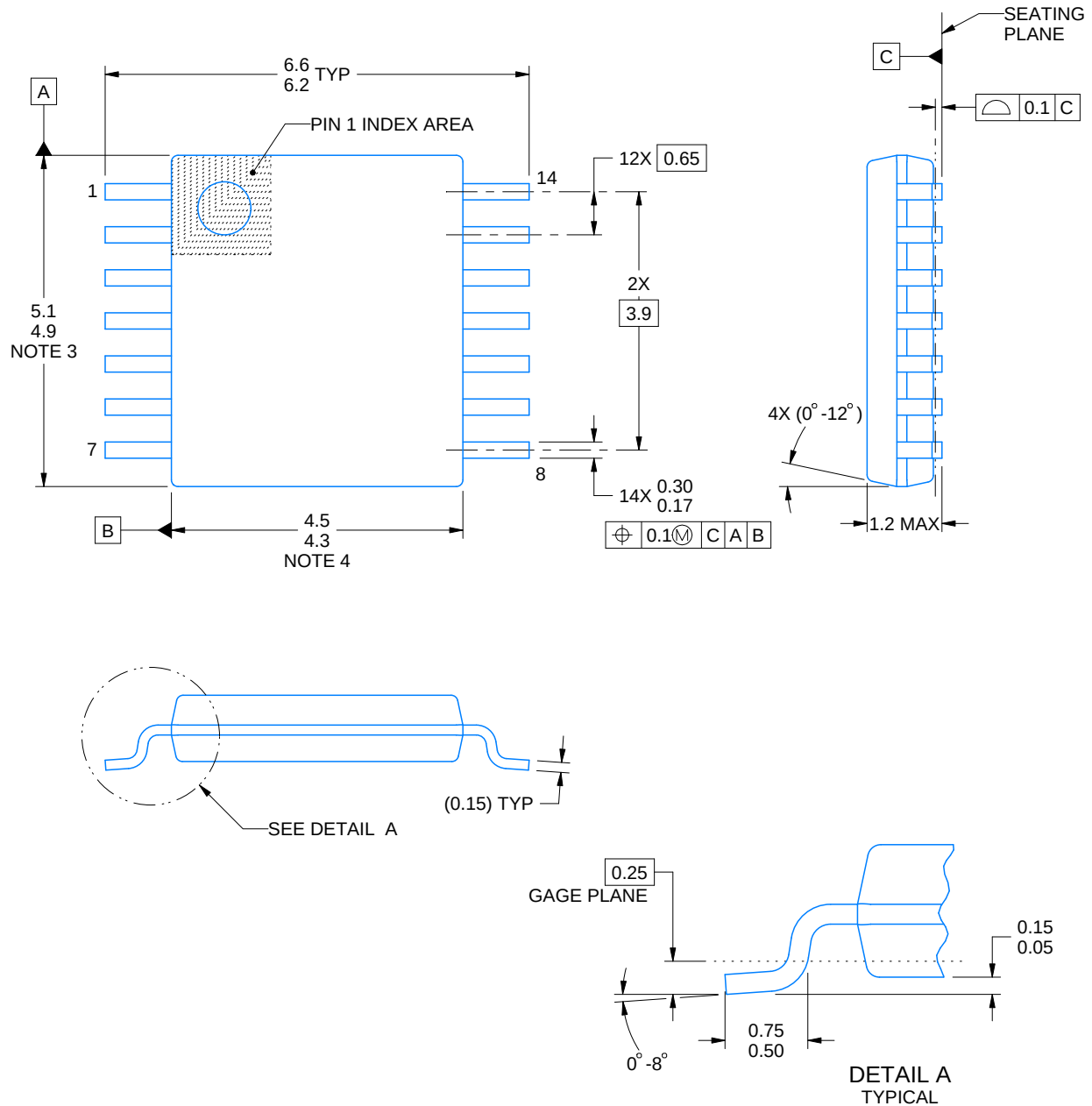
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

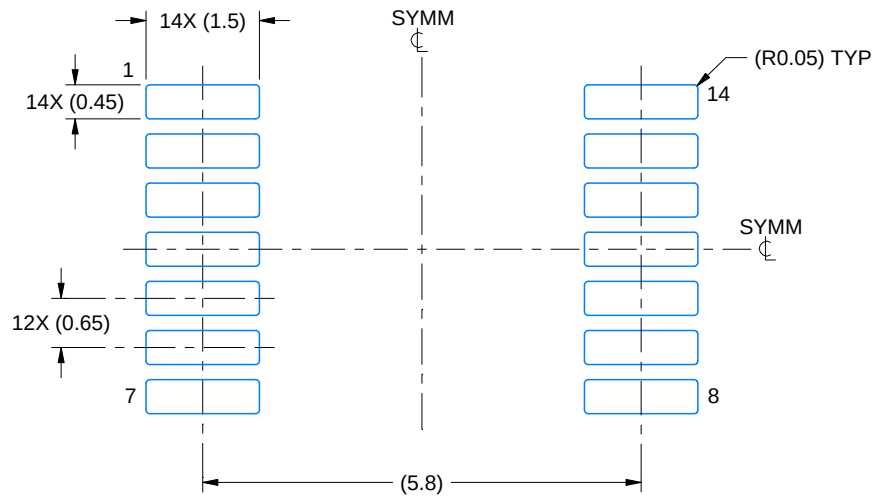
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

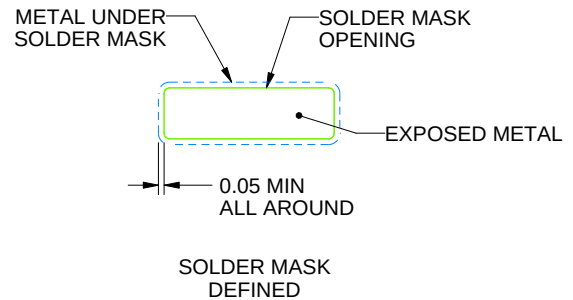
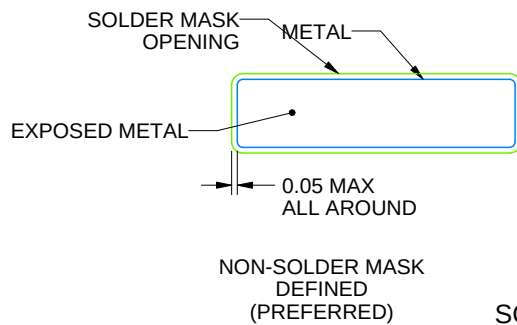
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

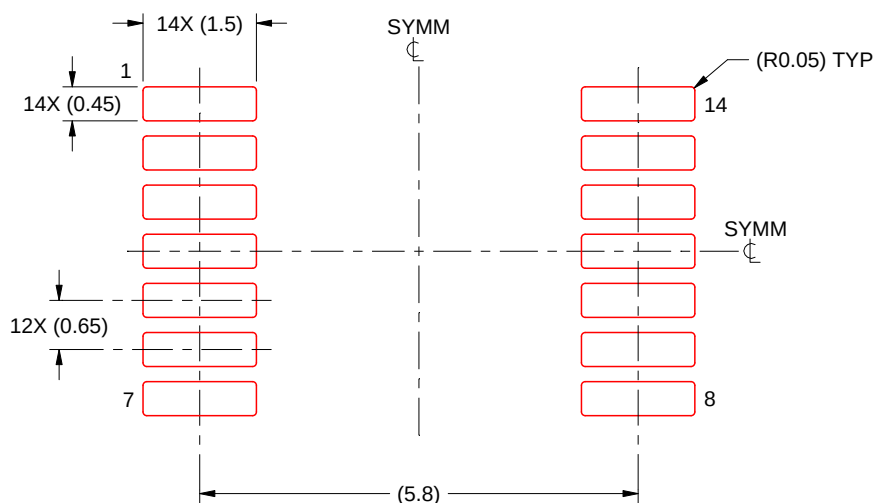
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月